

M62376GP

8-BIT 12CH D-A CONVERTER IC BUILT-IN 12-BIT I/O EXPANDER

DESCRIPTION

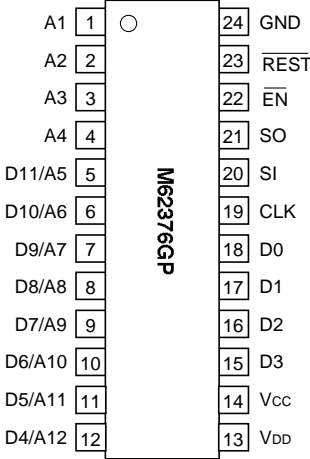
The M62376GP is a semiconductor IC that adopts a CMOS structure having 12-channel of 8-bit D-A converter and 12-bit I/O expander. The IC has achieved a wide operation range of 2.7V to 5.5V in power voltage.

Data is easily available via 3-wire combination system serial input of SI, CLK and \overline{EN} . The IC also provides an SO pin enabling cascade connection. It provides 8 pins that share D-A converter and I/O ports that can be arbitrarily switched with serial input data.

FEATURES

- Supply voltage 2.7 to 5.5V
- Adopts 4 special ports for each of DAC and I/O and 8 ports that share DAC output and I/O.
- Each port can be set by serial data for input/output status.
- Built-in power-on reset where D-A output is set to "L" in the initial status and I/O goes to Hi-impedance when power is turned on.
- Small package of 0.65mm pitch and 24 pin.

PIN CONFIGURATION (TOP VIEW)

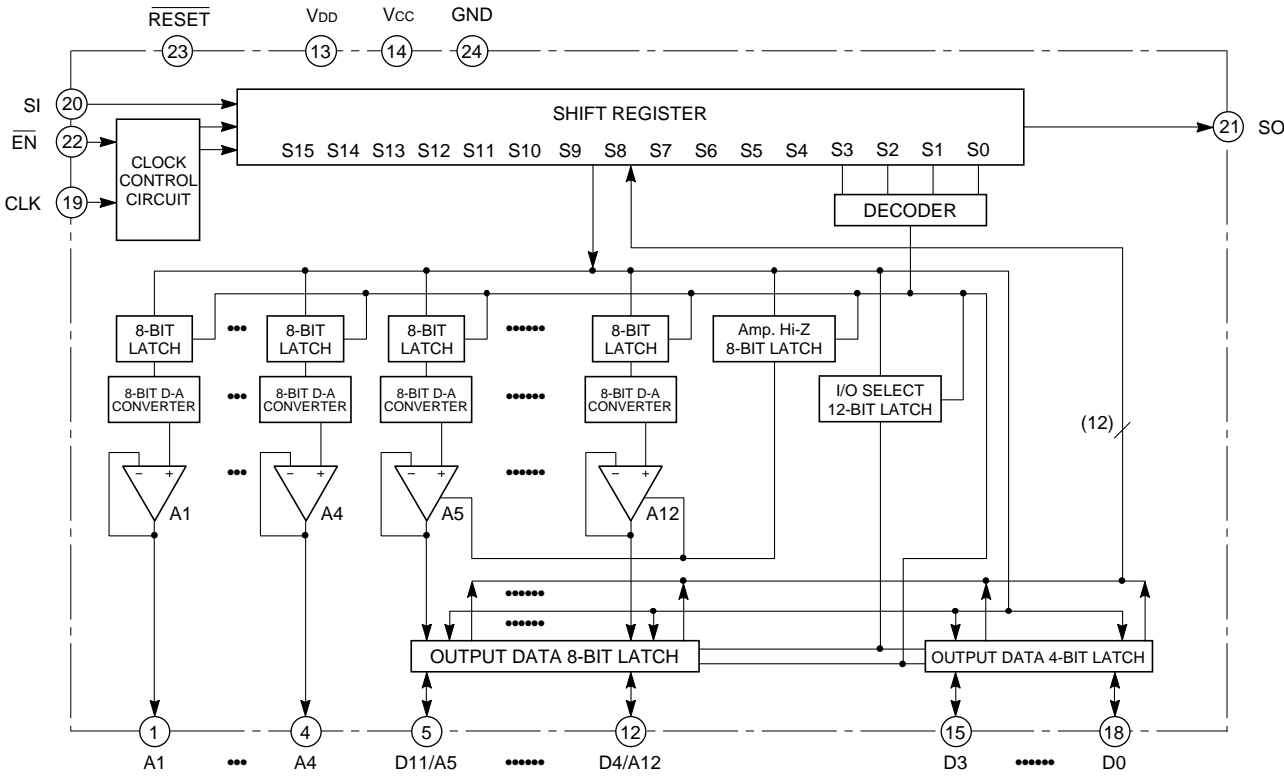


Outline 24P2E-A

APPLICATION

Adjustment/control of industrial or home-use electronic equipment, such as VCR camera, VCR set, TV, and CRT display.

BLOCK DIAGRAM



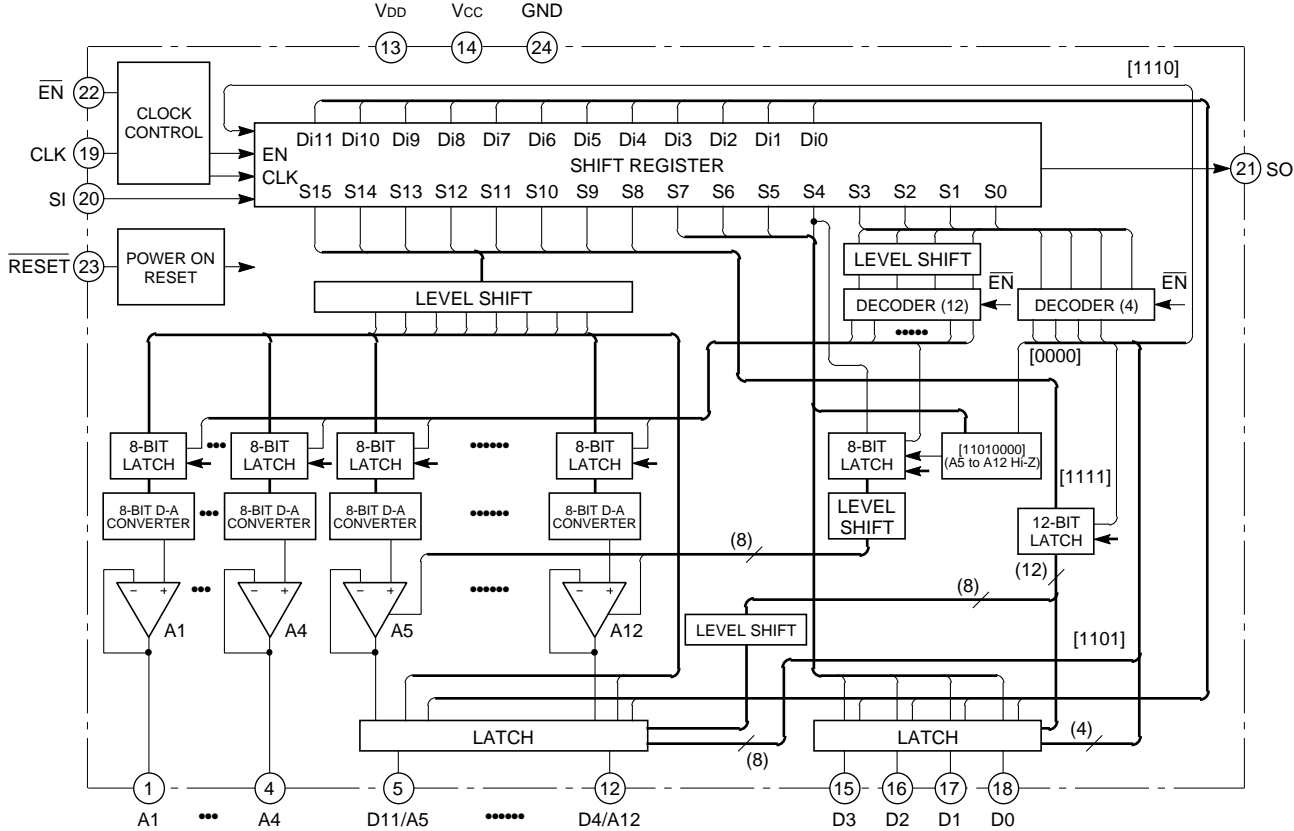
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EXPLANATION OF TERMINALS

Pin No.	Symbol	Function
⑳	SI	Serial data input pin. Enters serial data of 16-bit in length.
㉑	SO	Outputs data from 16-bit shift register that reads serial data or parallel data.
⑲	CLK	Shift clock input pin. At the rise of shift clock, input signal from the SI pin is entered into the 16-bit shift register.
㉒	$\overline{\text{EN}}$	Entry of low level into the $\overline{\text{EN}}$ pin starts to read data. Putting 16-bit data at high level after input loads the input data to a specified register.
①	A1	Special output pin for 8-bit D-A converter (DAC)
②	A2	
③	A3	
④	A4	
⑤	D11/A5	Pin that shares I/O and DAC output. Settings can be selected with serial data. D4 to D11 are connected to the V _{DD} power supply.
⑥	D10/A6	
⑦	D9/A7	
⑧	D8/A8	
⑨	D7/A9	
⑩	D6/A10	
⑪	D5/A11	
⑫	D4/A12	
⑱	D0	Digital input output pin.
⑰	D1	
⑯	D2	
⑮	D3	
⑭	V _{CC}	Digital block power supply pin.
㉔	GND	GND pin
⑬	V _{DD}	Power supply pin in analog block and reference voltage input pin on the upper side of D-A converter
㉓	$\overline{\text{RESET}}$	$\overline{\text{RESET}}$ pin

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EXPLANATION OF TERMINALS BLOCK DIAGRAM



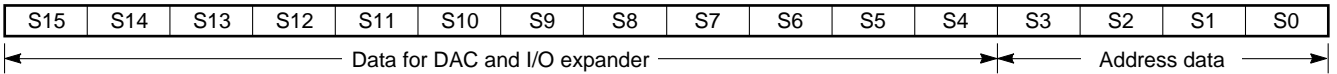
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DATA STRUCTURE

Serial data

MSB

LSB



Address data

S3	S2	S1	S0	Setup
0	0	0	0	(a)
0	0	0	1	A1 selection
0	0	1	0	A2 selection
0	0	1	1	A3 selection
0	1	0	0	A4 selection
0	1	0	1	A5 selection
0	1	1	0	A6 selection
0	1	1	1	A7 selection
1	0	0	0	A8 selection
1	0	0	1	A9 selection
1	0	1	0	A10 selection
1	0	1	1	A11 selection
1	1	0	0	A12 selection
1	1	0	1	I/O expander (serial → parallel conversion)
1	1	1	0	I/O expander (parallel → serial conversion)
1	1	1	1	I/O expander status setup

- I/O expander (serial → parallel conversion)
Outputs data on S4 to S15 to pins D0 to D11.

S3	S2	S1	S0
1	1	0	1

- I/O expander (parallel → serial conversion)
Writes data on D0 to D11 pins into S4 to S15.
When next data communication is provided, outputs data sequentially from S0 pin at the rise of the shift clock (CLK).

S3	S2	S1	S0
1	1	1	0

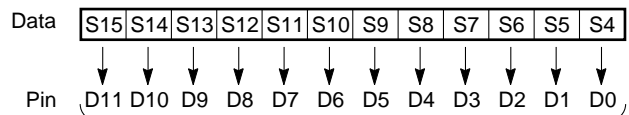
- I/O expander status setup register
Sets input/output pin of I/O expanders.

Data

"0": Input mode (Hi-Z status)

"1": Output mode

S3	S2	S1	S0
1	1	1	1



DAC data

S15	S14	S13	S12	S11	S10	S9	S8	S7	S6	S5	S4 ^(*)	Analog output voltage (Reference voltage on the lower side=0.0V fixed)
0	0	0	0	0	0	0	0	X	X	X	0	(V _{DD} /256)X1 [V] (1LSB)
0	0	0	0	0	0	0	1	X	X	X	0	(V _{DD} /256)X2 [V] (2LSB)
0	0	0	0	0	0	1	0	X	X	X	0	(V _{DD} /256)X3 [V] (3LSB)
∮	∮	∮	∮	∮	∮	∮	∮	∮	∮	∮	∮	∮
1	1	1	1	1	1	1	0	X	X	X	0	(V _{DD} /256)X255 [V] (255LSB)
1	1	1	1	1	1	1	1	X	X	X	0	V _{DD} [V] (256LSB)
X	X	X	X	X	X	X	X	X	X	X	1	High-impedance (I/O expander selected)

X :Don't care

(*): Only A5 to A12 outputs are available for DAC output by S4 and Hi-Z conversion.

(a) Command to set DAC output to High-impedance (DACHiZ command)

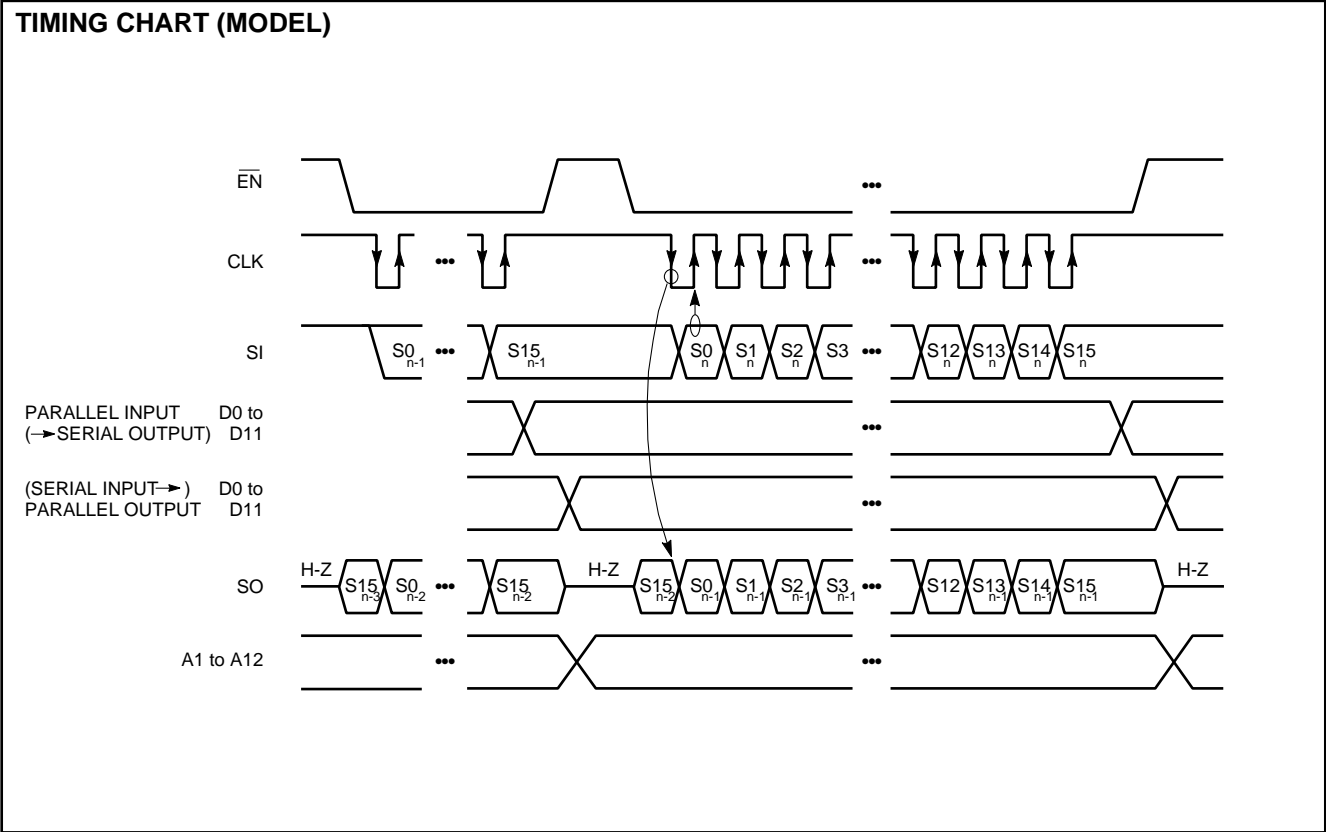
S15	S14	S13	S12	S11	S10	S9	S8	S7	S6	S5	S4	S3	S2	S1	S0	Analog output voltage
X	X	X	X	X	X	X	X	1	1	0	1	0	0	0	0	Sets D-A output of A5 to A12 to High-impedance.

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- (b) Initial status just after power is turned on:
 - Low level output from A1 to A4 (set to [00]h)
 - D4/A12 to D11/A5: DAC output of High-impedance (Hi-Z), I/O of input mode (Hi-Z)
 - D0 to D3 :input mode (Hi-Z)

- (c) The DACHiZ command is effective only for DAC settings (A5 to A12), but not for the I/O ports (D0 to D11)

Note: To change the status of pins D4/A12 to D11/A5, switch both analog and digital after setup of High-impedance.



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V _{CC}	Digital supply voltage		-0.3 to 7.0	V
V _{DD}	Analog supply (D-A converter upper reference voltage)		-0.3 to 7.0	V
V _{IN}	Input voltage	V _{CC} supply side pin	-0.3 to V _{CC} +0.3	V
V _{out}	Output voltage	V _{CC} supply side pin	-0.3 to V _{CC} +0.3	V
V _{IN}	Input voltage	V _{DD} supply side pin	-0.3 to V _{DD} +0.3	V
V _{out}	Output voltage	V _{DD} supply side pin	-0.3 to V _{DD} +0.3	V
P _d	Power dissipation		200	mW
T _{opr}	Operating temperature		-20 to +85	°C
T _{stg}	Storage temperature		-40 to +125	°C

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**ELECTRICAL CHARACTERISTICS
RECOMMENDED OPERATING CONDITION**

Symbol	Parameter	Conditions	Ratings	Unit
V _{CC}	Digital supply voltage		2.7 to 5.5	V
V _{DD}	Analog supply (D-A converter upper reference voltage)	V _{DD} V _{CC}	2.7 to 5.5	V
V _{IN}	Input pin voltage (V _{CC} part)	\overline{EN} , SI, D0 to D3	0 to V _{CC}	V
V _{OUT}	Output pin voltage (V _{CC} part)	SO, D0 to D3	0 to V _{CC}	V
V _{IN}	Input pin voltage (V _{DD} part)	RESET, D4/A12 to D11/A5	0 to V _{DD}	V
V _{OUT}	Output pin voltage (V _{DD} part)	A1 to A4, D4/A12 to D11/A5	0 to V _{DD}	V

DIGITAL PART [V_{CC}] (V_{CC}=2.7 to 5.5V, T_a=-20 to +85°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
V _{CC}	Supply voltage		2.7	3.0	5.5	V
I _{CC}	Supply current	CLK=1MHz operation, V _{CC} =3V, I _{AO} =0μA	-		2.5	mA
I _{ILK}	Input leak current	V _{IN} =0 to V _{CC}	-10		10	μA
V _{IL}	Input low voltage				0.2V _{CC}	V
V _{IH}	Input high voltage		0.5V _{CC}			V
V _{OL}	Output low voltage	I _{OL} =2.5mA			0.4	V
V _{OH}	Output high voltage	I _{OH} =-400μA	V _{CC} -0.4			V
V _{T+}	Forward threshold voltage (\overline{EN} , CLK)				0.5V _{CC}	V
V _{T-}	Backward threshold voltage (\overline{EN} , CLK)		0.2V _{CC}			V

DIGITAL PART [V_{DD}] (V_{DD}=2.7 to 5.5V, T_a=-20 to +85°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
V _{DD}	Supply voltage		2.7	3.0	5.5	V
I _{ILK}	Input leak current	V _{IN} =0 to V _{DD}	-10		10	μA
V _{IL}	Input low voltage				0.2V _{DD}	V
V _{IH}	Input high voltage		0.5V _{DD}			V
V _{OL}	Output low voltage	I _{OL} =2.5mA			0.4	V
V _{OH}	Output high voltage	I _{OH} =-400μA	V _{DD} -0.4			V

Note. For circuit current of V_{DD}, see the analog block.

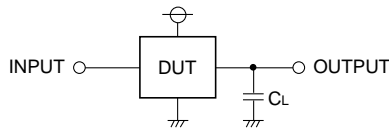
ANALOG PART (V_{DD} (V_{refU}) =2.7 to 5.5V, T_a=-20 to +85°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
I _{DD}	Dissipation current	V _{refU} =3V input data condition: When maximum current of R-2R rudder is supplied	-	1.5	3.5	mA
V _{DD} (V _{refU})	D-A converter upper reference voltage range	In the setup range of reference voltage, all values are not taken with output. Values to be taken depend on the item of buffer amplifier output voltage range.	2.7		5.5	V
V _{AO}	Buffer amplifier output voltage range	I _{AO} =±100μA	0.1		V _{DD} -0.1	V
		I _{AO} = +500μA -200μA	0.2		V _{DD} -0.2	
I _{AO}	Buffer amplifier output drive range	Upper side saturation voltage=0.4V Lower side saturation voltage=0.4V	-0.3		1	mA
S _{DL}	Differential nonlinearity error	V _{DD} =2.700V (V _{refU}) Without load (I _{AO} =+0μA)	-1.0		1.0	LSB
S _L	Nonlinearity error		-1.5		1.5	LSB
S _{ZERO}	Zero code error		-2.0		2.0	LSB
S _{FULL}	Full scale error		-2.0		2.0	LSB
C _O	Output capacitive load					10
R _O	Buffer amplifier output impedance			5		

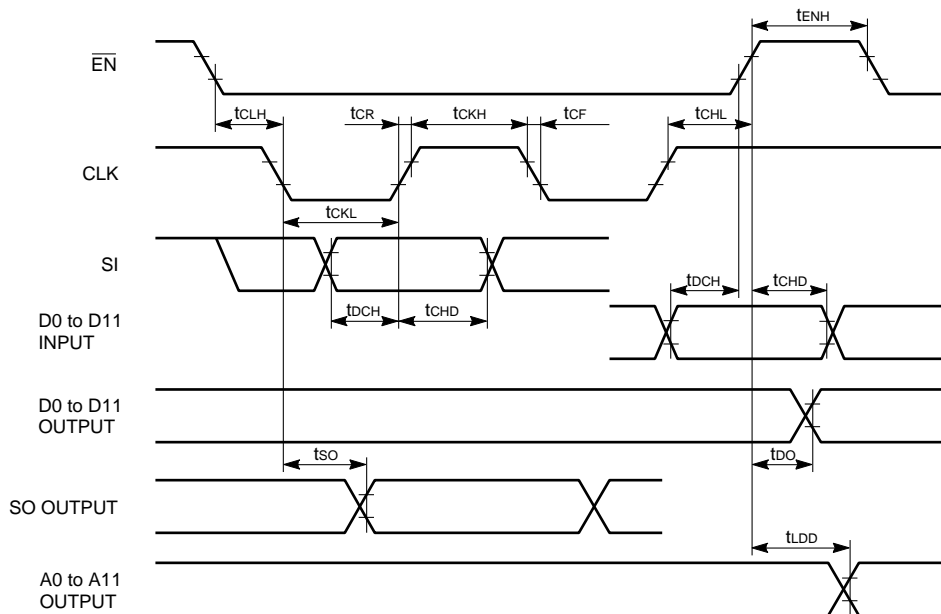
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AC ELECTRICAL CHARACTERISTICS ($V_{CC}, V_{DD}=2.7$ to $5.5V$, $T_a=-20$ to $+85^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
tCKL	Clock low pulse width		200			ns
tCKH	Clock high pulse width		200			ns
tCR	Clock rise time					
tCF	Clock fall time				200	ns
tdCH	Data setup time		30			ns
tCHD	Data hold time		60			ns
tCLH	Clock (\overline{EN}) setup time		100			ns
tCHL	\overline{EN} setup time		200			ns
tENH	\overline{EN} high hold time		200			ns
tSO	Serial data output delay time	$C_L=100pF$			350	ns
tDO	Parallel data output delay time	$C_L=100pF$			600	ns
tLDD	D-A output settling time	$C_L 100pF, V_{AO}:0.1 \rightarrow 2.6V$ Until output takes $\pm 2LSB$ of the final value.			100	μs

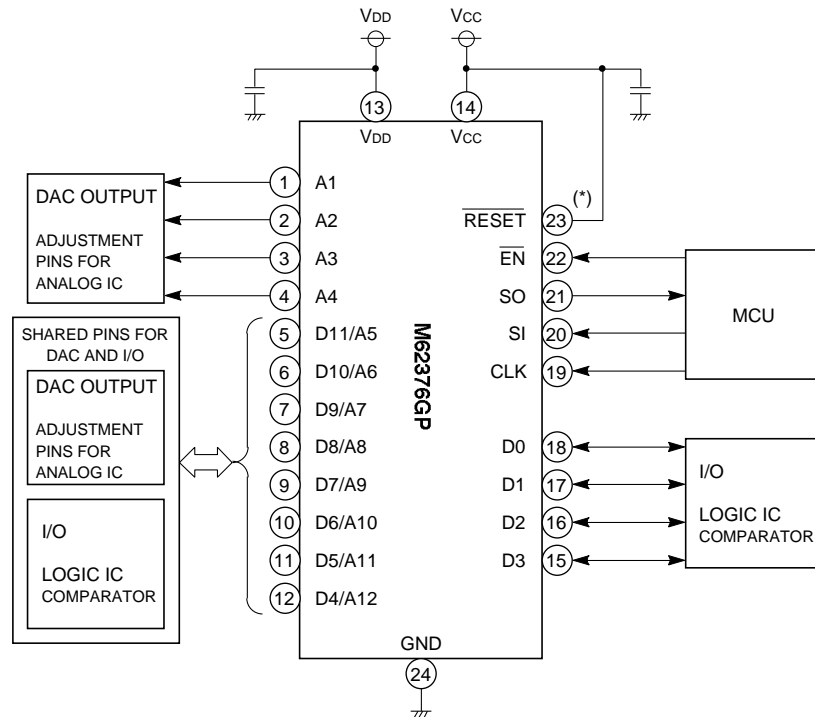


TIMING CHART



8-BIT 12CH D-A CONVERTER IC BUILT-IN 12-BIT I/O EXPANDER

APPLICATION EXAMPLE



PRECAUTION FOR USE

This IC has two power supply pins and a ground pin. Superimposition of these pins with ripple and spike noise may cause reduction of conversion accuracy and occurrence of malfunction. Be sure to insert a capacitor between each power supply and the GND pin to stabilize D-A converting operation.

The output buffer amplifier of this IC has strong characteristics against capacitive load. Accordingly, when the capacitance (10µF MAX.) is connected between output and ground to remove jitter and noise due to installation of output line, no problem may occur in operation of DAC. However, notice that the removal results in lengthening the settling time.

This IC also provides power-on reset function. To assure the resetting operation, power supply should be turned on in the order of timing shown in the diagram below.

(Order): 1. V_{CC} → 2. V_{DD}

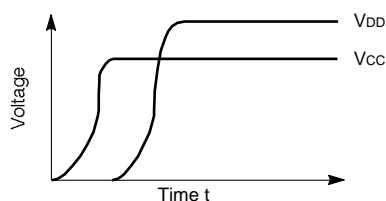


Fig. 1 Order for power-on

(*) The $\overline{\text{RESET}}$ pin is directly connected with the power pin to use power-on reset. However, when forced reset is done from outside, the capacitance (0.1 to 10µF) should be connected between $\overline{\text{RESET}}$ pin and ground to remove noise due to installation of line, etc.